



PATENT
(5500-97500/TT5529)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application No.: 10/653,754

Filed: September 3, 2003

Inventor(s):

Stephan G. Meier

S. Craig Nelson

Gene W. Shen

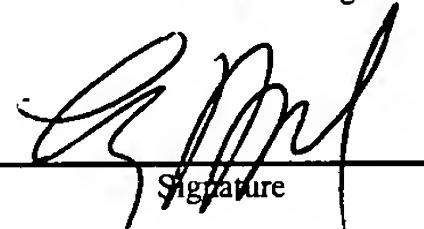
Title: Low Power Way-Predicted
Cache

§ Examiner: Unknown
§ Group/Art Unit: 2131
§ Atty. Dkt. No: 5500-97500
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I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on the date indicated below.

Lawrence J. Merkel

Name of Registered Representative


Signature

December 30, 2003

Date

INFORMATION DISCLOSURE STATEMENT

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Please incorporate the document listed on the attached Form PTO-1449 into the electronic Information Disclosure statement previously filed.

Applicant requests consideration of ☒ the references listed on the attached Form PTO-1449 and/or ☒ the additional information identified below in paragraph 3. A copy of each reference listed on the Form PTO-1449 is enclosed.

1. This Information Disclosure Statement is submitted:

- a. ☒ within 3 months of the filing date of a national application other than a continued prosecution application under § 1.53(d);
☐ within 3 months of the date of entry of the national stage as set forth in § 1.491 in an International application;
☒ before the mailing date of a first Office Action on the merits; or
☐ before the mailing of a first Office Action after the filing of a request for continued examination under § 1.114.

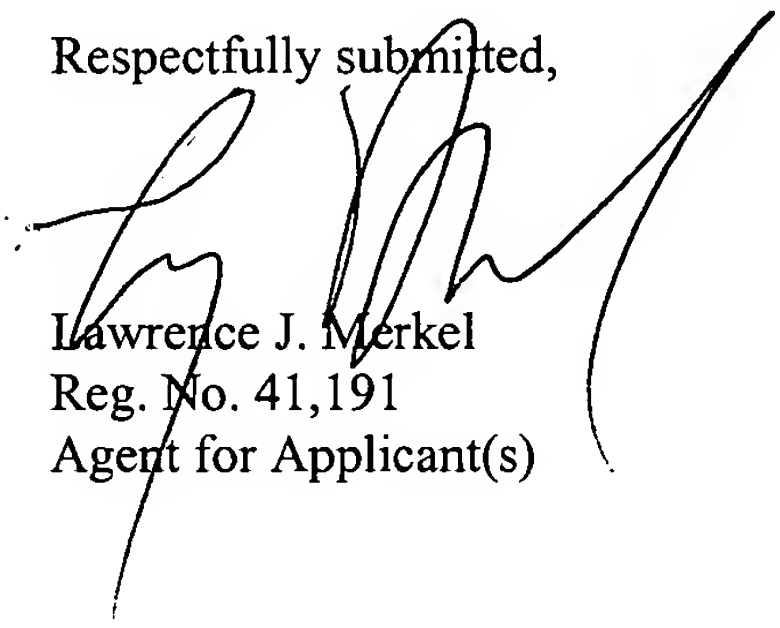
- b. ☐ after the events of above paragraph 1a and prior to the mailing date of a final Office Action or Notice of Allowance, and thus: ☐ the certification of paragraph 2 below is provided, or ☐ a fee of \$180.00 is enclosed.
- c. ☐ after the mailing date of a final Office Action or a Notice of Allowance and prior to payment of the issue fee, and thus: the certification of paragraph 2 below is provided and a fee of \$180.00 is enclosed.
2. It is hereby certified:
- ☐ that each item of information contained in this Information Disclosure Statement was cited in a communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the Statement, or
- ☐ that no item of information contained in the Information Disclosure Statement was cited in a communication from a foreign patent office in a counterpart foreign application or, to the knowledge of the person signing the certification after making reasonable inquiry, was known to any individual designated in § 1.56 (c) more than three months prior to the filing of the Statement.
3. ☒ Consideration of the following additional information (including any co-pending or abandoned U.S. applications, prior uses and/or sales, etc.) is requested:
- U.S. Patent Application Serial No. 10/653,749 (5500-97600)
U.S. Patent Application Serial No. 09/476,577 (5500-50600)
4. For each non-English language reference listed on the attached Form PTO-1449:
- ☐ reference is made to an English language translation submitted herewith, and/or
- ☐ reference is made to a foreign patent office search report (in the English language) submitted herewith, and/or
- ☐ reference is made to an English language translation of a foreign patent office search report submitted herewith, and/or
- ☐ reference is made to the concise explanation contained in the specification of the present application at page(s) _____, and/or
- ☐ reference is made to the concise explanation set forth below:
5. ☐ Applicant also offers the following comments for the Examiner's consideration:
6. ☐ Also enclosed is a copy of a foreign search report citing these references.
7. ☐ The listed documents were brought to the attention of the Applicant(s) after payment of the issue fee in the captioned case. The documents were cited in a communication from a foreign patent office in a counterpart foreign application

not more than three months prior to the filing of this Information Disclosure Statement. Applicant(s) request this Information Disclosure Statement and attached Form PTO-1449 be placed in the file of the captioned application.

8. ☐ Applicant(s) requests that the Information Disclosure Statement and attached Form PTO-1449 and references, which are being filed before the grant of the patent and pursuant to 37 C.F.R. § 1.97(i), be placed in the file of the captioned application.

If any required fees are missing, the Commissioner is authorized to charge said fees to Meyertons, Hood, Kivlin, Kowert & Goetzel, P.C. Deposit Account No. 50-1505/5500-97500/LJM.

Respectfully submitted,



Lawrence J. Merkel
Reg. No. 41,191
Agent for Applicant(s)

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P.O. Box 398
Austin, TX 78767-0398
(512) 853-8800

Date: December 30, 2003

Form PTO-1449 (modified)
List of Patents and Publications
For Applicant's Information
Disclosure Statement
 (Use several sheets if necessary)

ATTY. DKT. NO. 5500-97500

SERIAL NO. 10/653,754

APPLICANT: Meier, et al.

GROUP: 2131

FILING DATE: September 3, 2003

U.S. PATENT DOCUMENTS

EXAM. INITIALS	REF. DES.	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB CLASS	FILING DATE IF APPROPRIATE

FOREIGN PATENT DOCUMENTS

EXAM. INITIALS	REF. DES.	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB CLASS	TRANSLATION YES/NO
	A1	0459232	12/4/91	EP			
	A2	0259095	3/9/98	EP			
	A3	0675443	10/4/95	EP			
	A4	2 674 044	9/18/92	FR			
	A5	2263987	8/11/93	GB			
	A6	2263985	8/11/93	GB			
	A7	2281422	3/1/95	GB			
	A8	98/20421	5/14/98	WO			
	A9	0651321	5/3/95	EP			
	A10	0467152	1/22/92	EP			
	A11	0381471	8/8/90	EP			

OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)

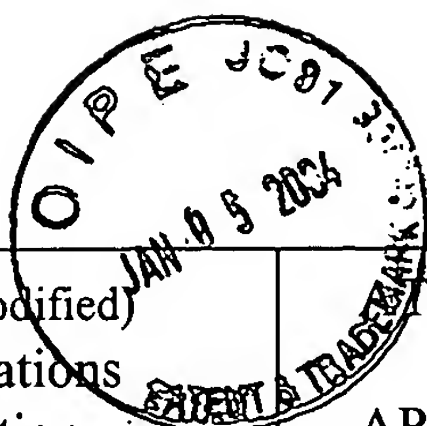
	A12	"Filtering Memory References to Increase Energy Efficiency," Kin, et al., IEEE Transactions on Computers, Vol. 49, No. 1, January 2000, 15 pages.
	A13	"Reducing Set-Associative Cache Energy via Way-Prediction and Selective Direct-Mapping," Powell, et al., IEEE, 2001, pp. 54-64.
	A14	"Low Load Latency Through Sum-Addressed Memory (SAM)," Lynch, et al., Sun Microsystems, Inc., 6 pages.
	A15	"The 16kB Single-Cycle Read Access Cache on a Next-Generation 64b Itanium Microprocessor," ISSCC 2002, Session 6, SRAM and Non-Volatile Memories, 6.6, 2 pages.
	A16	XP 000525181 Calder, et al, "Next Cache Line and Set Prediction," Department of Computer Science, University of Colorado, 8345 Computer Architecture News, May 23, 1995, No. 2, pp. 287-296.

EXAMINER:

DATE CONSIDERED:

EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to the patent owner.

Information Disclosure Statement--PTO 1449 (modified)



Form PTO-1449 (modified)
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For Applicant's Information
Disclosure Statement
(Use several sheets if necessary)

PATENT NO. 5500-97500

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FOREIGN PATENT DOCUMENTS

EXAM. INITIALS	REF. DES.	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB CLASS	TRANSLATION YES/NO

OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)

	A17	XP 000397920 Uchiyama, et al, "The Gmicro/500 Superscalar Microprocessor with Branch Buffers," 8207 IEEE Micro, October 13, 1993, No. 5, pp. 12-22.
	A18	Intel, "Chapter 2: Microprocessor Architecture Overview," pp. 2-1 through 2-4, 1994.
	A19	Slater, M., "AMD's Microprocessor K5 designed to Outrun Pentium" (Microprocessor Report, vol. 8, no. 14, October 24, 1994, 7 pages.
	A20	Rupley, et al, "P6: The Next Step?" PC Magazine, September 12, 1995, 16 pages.
	A21	Halfhill, "AMD K6 Takes on Intel P6," BYTE Magazine, January 1996, 4 pages.
	A22	Patterson, et al, "Computer Architecture: A Quantitative Approach," Section 8.3, pp. 408-425, published by Morgan Kaufmann Publishers, Inc., 1990.
	A23	Holstad, S., "Tutorial Tuesday: Decoding MMX" January 14, 1997, Earthlink Network, Inc. copyright 1997, 5 pages (see http://www.earthlink.net/daily/Tuesday/MMX)
	A24	"Intel Architecture Software Developer's Manual, Volume 1: Basic Architecture", Intel Corporation, Prospect IL, 1996, 1997, Chapter 8: Programming With The Intel MMX TM Technology, pp 8-1 through 8-15.
	A25	"Intel MMX TM Technology – Frequently Asked Questions" 6 pages (see http://www.intel.com/drg/mmx/support/faq/htm)
	A26	Patent Abstracts of Japan, Publication No. 07334423, published December 22, 1995.
	A27	Kessler et al., "Inexpensive Implementations of Set-Associativity," Computer Architecture Conference Proceedings, June 1989, pp. 131-139.

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